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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/989,931 6861326
Filing Date	November 21, 2001
First Named Inventor	Gonzalez et al.
Art Unit	2815
Examiner Name	Jose R. Diaz
Attorney Docket Number	MI22-1801

Total Number of Pages in This Submission

ENCLOSURES (*Check all that apply*)

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to a Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):

Return Receipt Postcard; Certificate of Correction (2);

Remarks

Additional Enclosures: Request for Certificate of Correction.

Patent No. 6,861,326 B2 Issued: March 1, 2005

Certificate MAY 30 2006 of Correction

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	David G. Latwesen, Ph.D., Reg. No. 38,533 Wells St. John, P.S.
Signature	
Date	5/22/06

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date:

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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, Washington, DC 20231.**

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MAY 30 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. 6,861,326 B2
Patent Issue Date ..... March 1, 2005
Application Serial No. 09/989,931
Filing Date ..... November 21, 2001
Assignee ..... Micron Technology, Inc.
Inventorship ..... Fernando Gonzalez et al.
Attorney's Docket No. MI22-1801
Title: Methods of Forming Semiconductor Circuitry

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PTO MISTAKE (37 C.F.R. 1.322(a))

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
ATTN: Decision and Certificate of Correction
Branch of the Patent Issue Division

From: David G. Latwesen, Ph.D. (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Sir:

It is hereby requested that a Certificate of Correction be issued with respect to Patent No. 6,861,326 B2, granted March 1, 2005, in accordance with the Certificate of Correction form attached hereto in duplicate.

The errors listed on the Certificate of Correction form were apparently incurred through the fault of the PTO as will be disclosed by the records of files in the Office.

Since this Certificate of Correction is being requested due to PTO errors, it is believed that no fee is due. However, in the event that a fee is required for issuance of this Certificate of Correction, please charge the fee specified under 37 C.F.R. § 1.20(a) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

05/26/2006 EAREGAY2 00000005 230925 6861326
01 FC:1811 100.00 DA

Attached hereto, in duplicate is Form PTO-1050, with at least one copy being suitable for printing.

Respectfully submitted,

Dated: 5/22/06

By: _____

David G. Latwesen, Ph.D.
Reg. No. 38,533

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,861,326 B2

DATED : March 1, 2005

INVENTOR(S) : Gonzalez et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, "References Cited", "U.S. PATENT DOCUMENTS",
Insert --4,903,108 2/1990 Young et al.
5,650,343 7/1997 Luning et al.--
Before "5,759,908".

Title Page, "References Cited", "U.S. PATENT DOCUMENTS",
Insert --6,306,691 B1 10/2001 Koh--
Before "6,358,806 B1".

Title Page, "References Cited", "U.S. PATENT DOCUMENTS",
Insert --6,566,210 B2 5/2003 Ajmera et al.--
Before "6,620,671 B1".

Title Page, "References Cited", "U.S. PATENT DOCUMENTS",
Insert --6,653,714 B2 11/2003 Matsuno et al.--
Before "2001/0008292 A1".

Title Page, "References Cited",
Insert --OTHER PUBLICATIONS
Lee, W. et al., "Investigation of Poly-$Si_{1-x}Ge_x$ for Dual-Gate CMOS Technology", IEEE Electron Device Letters, Vol. 19, No. 7, July 1998, pp. 247-249.
Wolf, S., "Silicon Processing for the VLSI Era: Vol. 1: Process Technology", 1986 Lattice Press, pp. 191-195.
Before "* cited by examiner".

Mailing Address of Sender:
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Patent No. 6,861,326 B2

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LIST OF ART CITED BY APPLICANT
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JUN 29 2004 JC42 PATENT & TRADEMARK OFFICE

ATTY. DOCKET NO.	SERIAL NO.
MI22-1801	09/989,931
APPLICANT: Fernando Gonzalez et al.	
FILING DATE Nov. 21, 2001 [RCE filed herewith]	GROUP 2815

U.S. PATENT DOCUMENTS

*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
✓	AA	6,653,714 B2	11/03	Matsuno et al.			
✓	AB	4,903,108	02/90	Young et al.			
✓	AC	6,566,210 B2	05/03	Ajmera et al.			
✓	AD	5,650,343	07/97	Luning et al.			
✓	AE	6,306,691 B1	10/01	Koh			
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AJ							
	AK							
	AL							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

✓	AM		Lee, W. et al., "Investigation of Poly-$Si_{1-x}Ge_x$ for Dual-Gate CMOS Technology", IEEE Electron Device Letters,
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✓	AN		Wolf, S., "Silicon Processing for the VLSI Era: Vol. 1: Process Technology", 1986 Lattice Press, pp. 191-195.
	AO		

EXAMINER [signature] DATE CONSIDERED 8/19/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

MAY 30 2006

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,861,326 B2

DATED : March 1, 2005

INVENTOR(S) : Gonzalez et al.

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Patent No. 6,861,326 B2

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LIST OF ART CITED BY APPLICANT
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ATTY. DOCKET NO.	SERIAL NO.
MI22-1801	09/989,931

APPLICANT: Fernando Gonzalez et al.

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